CLAIMS

[1] A method for manufacturing a solid-state imaging device in which an imaging region in which a plurality of unit pixels are arranged is provided on a semiconductor substrate, each of the unit pixel including a plurality of element formation regions and an element isolation formation region located between the plurality of element formation regions, the method comprising:

a step (a) of forming, on the semiconductor substrate, a protection film including an opening portion that exposes the element isolation formation region and a region located beside the element isolation formation region of the semiconductor substrate;

a step (b) of forming a sidewall on a side face of the opening in the protection film;

a step (c) of forming a trench in the element isolation formation region in the semiconductor substrate by etching using the protection film and the sidewall as a mask; and

a step (d) of forming an element isolation region by burying the trench with a burying film.

[2] The method for manufacturing a solid-state imaging device of Claim 1,

wherein the element formation regions of the semiconductor substrate include a n-type impurity, and

the method further comprising the step of implanting a p-type ion into a surface portion of the trench in the semiconductor substrate after the step (c) and before the step (d).

[3] The method for manufacturing a solid-state imaging device of Claim 1, further comprising the step of:

oxidizing a surface portion of the trench in the semiconductor substrate after the step (c) and before the step (d).

[4] The method for manufacturing a solid-state imaging device of Claim 1,

wherein in the step (a), a first insulating film and a second insulating film provided

on the first insulating film and having a property of oxidization resistance are formed as the protection film.

[5] The method for manufacturing a solid-state imaging device of Claim 1,

wherein in the step (d), the burying film is deposited by CVD.

[6] The method for manufacturing a solid-state imaging device of Claim 1,

wherein in the step (d), a level of the element isolation is allowed to be higher than an upper face of the semiconductor substrate by removing the protection film deeper than the burying film after the burying film is formed so as to bury the opening of the protection film.

[7] The method for manufacturing a solid-state imaging device of Claim 1,

wherein a peripheral circuit region including a drive circuit for operating the imaging region is provided beside the imaging region in the semiconductor substrate, and

an element isolation of the peripheral circuit region is formed by the same step as the step of forming the element isolation of the imaging region.

[8] The method for manufacturing a solid-state imaging device of Claim 7,

wherein in the peripheral circuit, only a NMOS transistor, only a PMOS transistor, or a CMOS transistor is formed.

[9] A method for manufacturing a solid-state imaging device in which an imaging region in which a plurality of unit pixels are arranged is provided on a semiconductor substrate, each of the unit pixel including a plurality of element formation regions and an element isolation formation region located between the plurality of element formation regions, the method comprising:

a step (a) of forming, on the semiconductor substrate, a protection film including an opening portion that exposes at least a part of the element isolation formation region of the semiconductor substrate;

a step (b) removing and patterning the part of the element isolation formation region of the semiconductor substrate by etching using the protection film as a mask after

the step (a);

a step (c) of forming an oxide film for element isolation by oxidizing a surface portion of the patterned element isolation formation region of the semiconductor substrate after the step (b); and

a step (d) of removing at least a part of the protection film after the step (c).

[10] The method for manufacturing a solid-state imaging device of Claim 9,

wherein in the step (a), a pad insulating film and an anti-oxidizing film located above the pad insulating film are formed as the protection film.

[11] The method for manufacturing a solid-state imaging device of Claim 10,

wherein in the step (a), an oxidizing film is interposed between the padding insulating film and the anti-oxidizing film.

[12] The method for manufacturing a solid-state imaging device of Claim 9,

wherein after the step (c), a part of the oxide film for element isolation is removed by etching.

[13] The method for manufacturing a solid-state imaging device of Claim 10,

wherein in the step (c), a bird's beak is formed in a surface portion of the semiconductor substrate, and

a part of the bird's beak is removed after the step (c).

[14] The method for manufacturing a solid-state imaging device of Claim 9,

wherein a n-type impurity is included in the element formation regions of the semiconductor substrate, and

the method further comprising the step of implanting a p-type ion into a surface portion of the patterned element isolation formation region of the semiconductor substrate after the step (b) and before the step (c).

[15] The method for manufacturing a solid-state imaging device of Claim 9,

wherein in the step (a), a width of the opening portion is narrower than a width of the element isolation formation region.

[16] The method for manufacturing a solid-state imaging device of Claim 9,

wherein in the step (d), a level of the element isolation formation region is allowed to be higher than an upper face of the semiconductor substrate by removing the protection film to a level deeper than an upper face of the oxide film for element isolation.

[17] The method for manufacturing a solid-state imaging device of Claim 9,

wherein a peripheral circuit region including a drive circuit for operating the imaging region is provided beside the imaging region in the semiconductor substrate, and

an element isolation region of the peripheral circuit region is formed by the same step as a step of forming an element isolation region of the imaging region.

[18] The method for manufacturing a solid-state imaging device of Claim 7,

wherein in the peripheral circuit region, only a NMOS transistor, only a PMIS transistor, or a CMOS transistor is formed.

[19] A method for manufacturing a solid-state imaging device in which an imaging region in which a plurality of unit pixels are arranged is provided on a semiconductor substrate, each of the unit pixel including a plurality of element formation regions and an element isolation formation region located between the plurality of element formation regions, the method comprising:

a step (a) of forming, on the semiconductor substrate, a protection film including an opening portion that exposes the element isolation formation region of the semiconductor substrate;

a step (b) of forming a trench by removing a part of the element isolation formation region of the semiconductor substrate by etching using the protection film as a mask;

a step (c) of removing the protection film after the step (b); and

a step (d) of performing thermal treatment in an atmosphere including hydrogen at a temperature in a range between 1000°C and 1300°C, both inclusive, after the step (b).

[20] The method for manufacturing a solid-state imaging device of Claim 19,

wherein in the step (d), a semiconductor film of a semiconductor material composing the semiconductor substrate is formed so as to cover an upper part of the trench by the thermal treatment, and

the method further comprising: a step (e) of implanting an impurity having a conductivity type different from that of the element formation regions into the semiconductor film after the step (d).

[21] The method for manufacturing a solid-state imaging device of Claim 19,

wherein in the step (d), a semiconductor film of a semiconductor material composing the semiconductor substrate is formed so as to cover an upper part of the trench by the thermal treatment, and

the method further comprising: a step (f) of oxidizing the semiconductor film after the step (d).

[22] The method for manufacturing a solid-state imaging device of Claim 19, further comprising:

a step (g) of subjecting a side face portion of the trench in the semiconductor substrate to thermal oxidation after the step (b) and before the step (d).

[23] The method for manufacturing a solid-state imaging device of Claim 19, further comprising:

a step (h) of forming an insulating film on a side face of the trench after the step (b) and before the step (d).

[24] The method for manufacturing a solid-state imaging device of Claim 19,

wherein a part of the element formation regions of the semiconductor substrate includes a n-type impurity,

the method further comprising:

a step (i) of implanting a p-type ion into a surface portion of the trench in the semiconductor substrate after the step (b) and before the step (d).

[25] The method for manufacturing a solid-state imaging device of Claim 19,

wherein a peripheral circuit region including a drive circuit for operating the imaging region is provided beside the imaging region in the semiconductor substrate, and

an element isolation region of the peripheral circuit region is formed by the same step as a step of forming an element isolation region of the imaging region.

[26] The method for manufacturing a solid-state imaging device of Claim 25,

wherein in the peripheral circuit region, only a NMOS transistor, only a PMOS transistor, or a CMOS transistor is formed.

[27] A method for manufacturing a solid-state imaging device in which an imaging region in which a plurality of unit pixels are arranged is provided on a semiconductor substrate, each of the unit pixel including a plurality of element formation regions and an element isolation formation region located between the plurality of element formation regions, the method comprising:

a step (a) of forming, on the semiconductor substrate, a protection film including an opening portion that exposes a part of the element isolation formation region of the semiconductor substrate;

a step (b) of forming a trench having a depth two time larger than a width thereof by removing a part of the element isolation formation region of the semiconductor substrate by etching using the protection film as a mask; and

a step (c) of forming a TEOS film for burying the trench by CVD after the step (b).

[28] The method for manufacturing a solid-state imaging device of Claim 27, further comprising:

a step (d) of subjecting a side face portion of the trench in the semiconductor substrate to thermal oxidation after the step (b) and before the step (c).

[29] The method for manufacturing a solid-state imaging device of Claim 27, further comprising:

a step (e) of forming an insulting film on a side face of the trench after the step (b) and before the step (c).

[30] The method for manufacturing a solid-state imaging device of Claim 27,

wherein a n-type impurity is included in a part of the element formation regions of the semiconductor substrate,

the method further comprising:

a step (f) of implanting a p-type ion into a part of a surface portion of the trench in the semiconductor substrate after the step (b) and before the step (c).

[31] The method for manufacturing a solid-state imaging device of Claim 27,

wherein a peripheral circuit region including a drive circuit for operating the imaging region is provided beside the imaging region in the semiconductor substrate, and

an element isolation region of the peripheral circuit region is formed by the same step as a step of forming an element isolation region of the imaging region.

[32] The method for manufacturing a solid-state imaging device of Claim 31,

in the peripheral circuit region, only a NMOS transistor, only a PMOS transistor, or a CMOS transistor is formed.

[33] A method for manufacturing a solid-state imaging device provided with, on a semiconductor substrate, an imaging region in which a plurality of unit pixels respectively including photoelectric conversion sections and active regions are arranged,

wherein in a step of forming an element isolation trench between the photoelectric conversion sections and between the respective photoelectric conversion regions and the respective active regions in the semiconductor substrate, a wall of the element isolation trench is tapered.

[34] A method for manufacturing a solid-state imaging device provided with, on a semiconductor substrate, an imaging region in which a plurality of unit pixels respectively including photoelectric conversion sections and active regions are arranged,

wherein in a step of forming an element isolation trench between the photoelectric conversion sections and between the respective photoelectric conversion regions and the respective active regions in the semiconductor substrate, an angle between a wall face of

the element isolation trench and a surface of the semiconductor substrate is set within a range between 110° and 130°, both inclusive.

[35] The method for manufacturing a solid-state imaging device of Claim 33 or 34, comprising the step of, after a first insulating film and a second insulting film different in kind from the first insulating film are deposited on the semiconductor substrate sequentially, pattering the first insulating film and the second insulating film before the step of forming the element isolation trench,

wherein the step of forming the element isolation trench includes a step of etching the semiconductor substrate using the patterned first insulting film and the patterned second insulating film as a mask.

[36] The method for manufacturing a solid-state imaging device of Claim 35,

wherein in the step of etching the semiconductor substrate, a flow rate of an oxygen gas is set to be 5 % or lower of a flow rate of a chlorine gas.

[37] The method for manufacturing a solid-state imaging device of Claim 33 or 34,

wherein if a conductive type of the photoelectric conversion sections is n-type, a step of forming a p-type semiconductor layer at at least a part in contact with the element isolation trench in a region of the semiconductor substrate to be the photoelectric conversion sections is provided after the step of forming the element isolation trench,

while if a conductive type of the photoelectric conversion sections is p-type, a step of forming a n-type semiconductor layer at at least a part in contact with the element isolation trench in a region of the semiconductor substrate to be the photoelectric conversion sections is provided after the step of forming the element isolation trench.

[38] The method for manufacturing a solid-state imaging device of Claim 33 or 34,

wherein the solid-state imaging device includes, on the semiconductor substrate, a peripheral circuit region including a drive circuit for operating the imaging region, and

element isolation structures are formed simultaneously in the peripheral circuit region and the imaging region.

[39] The method for manufacturing a solid-state imaging device of Claim 33 or 34,

wherein the solid-state imaging device includes, on the semiconductor substrate, a peripheral circuit region including a drive circuit for operating the imaging region, and

different element isolation structures are formed in the peripheral circuit region and the imaging region.

[40] The method for manufacturing a solid-state imaging device of Claim 33 or 34,

wherein only a NMOS transistor or only a PMOS transistor is used as a transistor provided in the peripheral circuit region.

[41] The method for manufacturing a solid-state imaging device of Claim 33 or 34,

wherein a CMOS transistor is used as a transistor provided in the peripheral circuit region.

[42] A solid-state imaging device in which an imaging region in which a plurality of unit pixels are arranged is provided on a semiconductor substrate, each of the unit pixels including a plurality of element formation regions and an element isolation formation region located between the plurality of element formation regions,

wherein in the element isolation formation region, a trench is formed in a part of the semiconductor substrate and a burying film is provided for burying the trench, and

the trench is formed by removing a part of the semiconductor substrate using a protection film which covers the element formation regions of the semiconductor substrate and which includes an opening portion that exposes the element isolation formation region of the semiconductor substrate and a sidewall provided on a side face of the opening portion in the protection film as a mask.

[43] The solid-state imaging device of Claim 42,

wherein a n-type impurity is included in the element formation regions of the semiconductor substrate, and

a p-type impurity is included in a surface portion of the trench in the element isolation formation region of the semiconductor substrate.

[44] The solid-state imaging device of Claim 42,

wherein a silicon oxide film is provided on a surface of the trench.

[45] The solid-state imaging device of Claim 42,

wherein a level of the burying film is higher than an upper face of the semiconductor substrate.

[46] A solid-state imaging device in which an imaging region in which a plurality of unit pixels are arranged is provided on a semiconductor substrate, each of the unit pixels including a plurality of element formation regions and an element isolation region located between the plurality of element formation regions,

wherein a part of the element isolation region of the semiconductor substrate is patterned, and

an oxide film for element isolation that buries the patterned element isolation region, which is obtained by oxidizing a part of the semiconductor substrate which is exposed at a surface of the patterned element isolation region is provided.

[47] The solid-state imaging device of Claim 46,

wherein a n-type impurity is included in the element formation regions of the semiconductor substrate, and

a p-type impurity is included in a surface portion of a concave in the semiconductor substrate in the element isolation region of the semiconductor substrate.

[48] The solid-state imaging device of Claim 46,

wherein a level of the oxide film for element isolation is higher than an upper face of the semiconductor substrate.

[49] A camera characterized by using the solid-state imaging device of Claim 46.

[50] A solid-state imaging device in which an imaging region in which a plurality of unit pixels are arranged is provided on a semiconductor substrate, each of the unit pixels including a plurality of element formation regions and an element isolation region located between the plurality of element formation regions,

wherein in the element isolation region, a trench located in an upper part of the semiconductor substrate is formed, an element isolation film electrically isolating between the plurality of element formation regions is provided so as to cover at least an upper part of the trench, and a cavity is formed at a part within the trench.

[51] The solid-state imaging device of Claim 50,

wherein the element isolation film covers an upper part of the cavity and includes a p-type impurity.

[52] The solid-state imaging device of Claim 50,

wherein the element isolation film is a silicon oxide film that covers an upper part of the cavity.

[53] The solid-state imaging device of Claim 50,

wherein the element isolation film is a TEOS film that buries the trench, and

the cavity is formed within a part of the of the TEOS film.

[54] A camera characterized by using the solid-state imaging device of Claim 50.

[55] A solid-state imaging device comprising:

a semiconductor substrate; and

an imaging region provided on the semiconductor substrate in which a plurality of unit pixels respectively including photoelectric conversion sections and active regions are arranged,

wherein an element isolation trench is formed between the photoelectric conversion sections and between the respective photoelectric conversion sections and the respective active regions, the element isolation trench having a tapered wall.

[56] A solid-state imaging device comprising:

a semiconductor substrate; and

an imaging region provided on the semiconductor substrate in which a plurality of unit pixels respectively including photoelectric conversion sections and active regions are arranged,

wherein an element isolation trench is formed between the photoelectric conversion sections and between the respective photoelectric conversion sections and the respective active regions, a wall face of the element isolation trench forming an angle within a range between 110° and 130°, both inclusive, with respect to a surface of the semiconductor substrate.

[57] The solid-state imaging device of Claim 55 or 56,

wherein if a conductive type of the photoelectric conversion sections is n-type, a p-type semiconductor layer is provided at at least a part in contact with the element isolation trench in a region of the semiconductor substrate to be the photoelectric conversion sections,

while if a conductive type of the photoelectric conversion sections is p-type, a n-type semiconductor layer is provided at at least a part in contact with the element isolation trench in a region of the semiconductor substrate to be the photoelectric conversion sections.

[58] The solid-state imaging device of Claim 55 or 56, further comprising:

a peripheral circuit region including a drive circuit for operating the imaging region in the semiconductor substrate,

wherein the peripheral circuit region and the imaging region have the same element isolation structure.

[59] The solid-state imaging device of Claim 55 or 56, further comprising:

a peripheral circuit region including a drive circuit for operating the imaging region in the semiconductor substrate,

wherein the peripheral circuit region and the imaging region have different element isolation structures.

[60] The solid-state imaging device of Claim 58 or 59,

wherein a transistor provided in the peripheral circuit region is only a n-type MOS transistor or only a p-type MOS transistor.

[61] The solid-state imaging device of Claim 58 or 59,

wherein a transistor provided in the peripheral circuit region is a COMS transistor.

[62] A camera characterized by using the solid-state imaging device of Claim 55 or 56.